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(54) **Polycrystalline silicon layers for semiconductor devices**

(57) Semiconductor devices containing one or more layers of polycrystalline silicon having a root means square roughness of not more than 20 angstroms are made by forming the silicon layers in the amorphous state by low pressure chemical vapor deposition in the temperature range 560—580°C and annealing to convert them to the polycrystalline state. The layers so formed are superior in smoothness lack of strain and precision of photolithographic definition to layers of silicon formed in the polycrystalline state. An interconnect 24 may be produced.

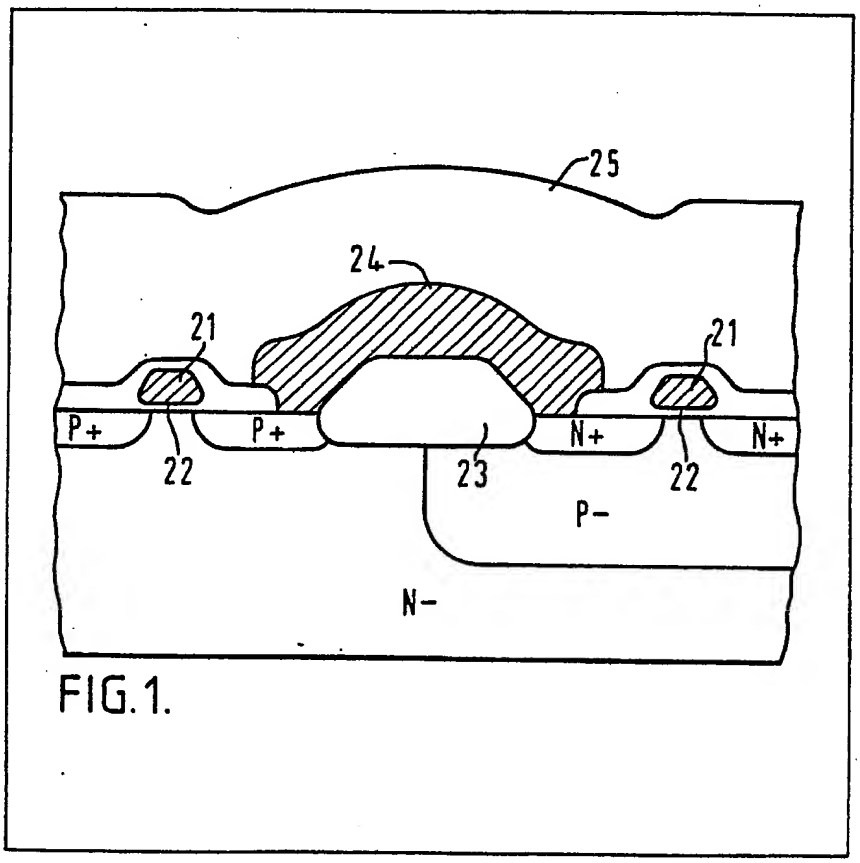

FIG.1.

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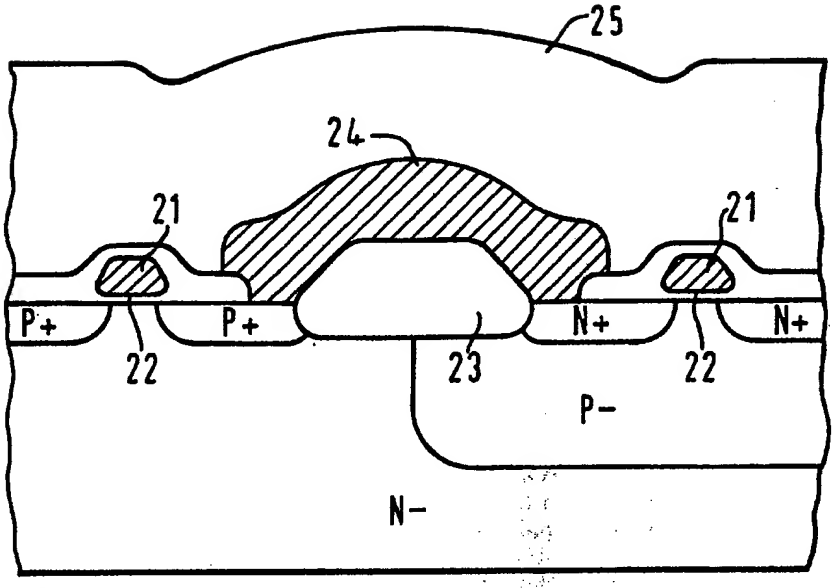
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24
21
21
P+
P+
N+
N+
22
23
22
P-
N-

FIG. 1.

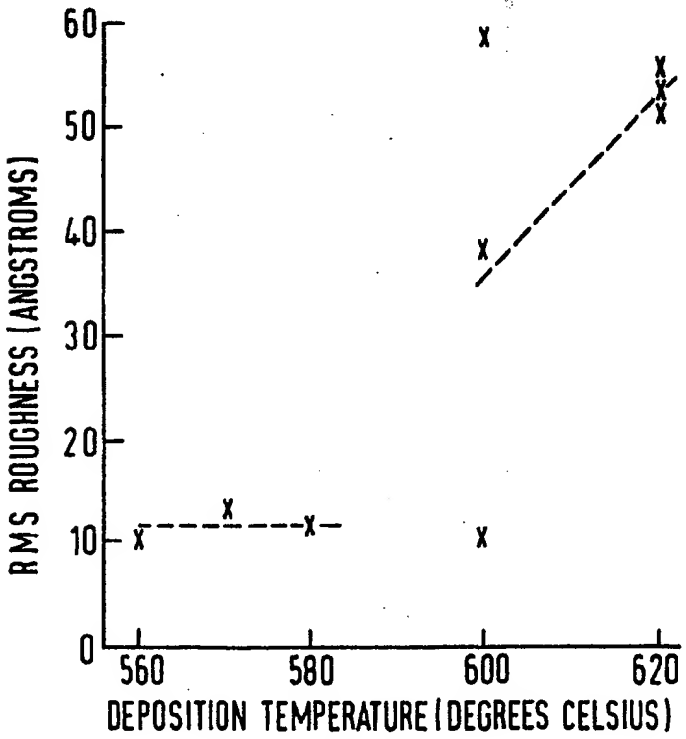
60
50
40
30
20
10
0
RMS ROUGHNESS (ANGSTROMS)
560
580
600
620
DEPOSITION TEMPERATURE (DEGREES CELSIUS)

FIG. 2.

SPECIFICATION

Polycrystalline silicon layers for semiconductor devices

This invention pertains to polycrystalline silicon layers in semiconductor devices and structures, particularly integrated circuit devices and structures.

The presence of one or a plurality of polycrystalline layers in semiconductor devices, particularly integrated circuit structures, is known. As such devices have become smaller and increasingly complex in design, there has been a corresponding increase in vertical structuring of multiple layers of various materials. Such devices often contain a plurality of layers of polycrystalline silicon which, in whole or in part, may be patterned, doped with various materials, oxidized to form an overlying layer of silicon dioxide or the like.

As the design requirements for semiconductor structures and devices become increasingly stringent, it is necessary that the individual layers be thinner, more uniform in properties and smoother. When a layer of dielectric material, such as silicon dioxide, is sandwiched between two conducting layers, either or both of which is polycrystalline silicon with rough surfaces, an electric field applied to the structure can localize and concentrate at surface asperities on the conducting layers, creating much stronger electric fields and rupturing the adjacent dielectric layer. More important, it has been demonstrated that it is easier for current to pass from one conducting layer to the next through an intervening dielectric layer at a "bump" or surface asperity in one or both conducting layers. Over a period of time, these phenomena will cause dielectric breakdown. Thus, it is desirable that the polycrystalline silicon layer be as smooth as possible.

In addition to very stringent requirements concerning smoothness, the polycrystalline silicon layers in complex integrated circuit devices must have little strain, have good crystalline perfection within the individual grains, and have a surface smoothness and homogeneity of grain structure suitable for the fine pattern lithography necessary for the fabrication of integrated circuits.

The growth of silicon in the amorphous or amorphous/polycrystalline state is known. It is likewise known that annealing such films at between about 850° and 1000°C. will convert them to the polycrystalline state. Conventionally, however, polycrystalline layers formed in the manufacture of semiconductor devices are formed in the polycrystalline state. This is because silicon layers can be formed in the polycrystalline state in considerably less time than in the amorphous state, and amorphous formed layers are considered by some experts to be comparatively unstable. In addition, the requirements for such devices have, in the past, been such that layers formed in the polycrystalline state were acceptable. However, silicon layers formed in the polycrystalline state will, in all probability, not be able to meet the requirements of thinness and smoothness for complex multilayer semiconductor devices of the future.

It has been found in accordance with this invention that complex, multilayer semiconductor devices are markedly improved by forming the silicon layers therein in the amorphous state and annealing to the polycrystalline state.

Multilayer, complex semiconductor and other electronic devices containing one or more layers of polycrystalline silicon are improved by providing such layers with an exceptional surface smoothness, crystalline perfection and microhomogeneity by growing them in the amorphous state and annealing to convert them to the polycrystalline state. Surprisingly, the exceptional smoothness is retained in the polycrystalline layer.

In the drawing:

FIGURE 1 is a cross-sectional view of an interconnection device containing a plurality of polycrystalline silicon layers.

FIGURE 2 is a graph of root mean square surface roughness of annealed polycrystalline silicon films as a function of deposition temperature.

The present invention relates to semiconductor or other electronic devices which contain one or more layers of polycrystalline silicon. Such devices or structures commonly contain or are part of an electronic circuit. Examples of such devices include MOS gates, interconnects, load resistors, double polycrystalline silicon capacitors and numerous devices found in the high-density integrated circuit technology. As utilized herein, the term "device" shall include semiconductor structures or assemblies. In general, this invention is applicable to any electronic device requiring one or more layers of polycrystalline silicon, such as that illustrated in FIG. 1. Although the present invention will improve a single layer of polycrystalline silicon on the surface of a device, the unexpected advantages thereof are principally realized with an internal layer or layers in a multilayer structure.

In FIG. 1, an interconnect device, e.g., between two transistors (not shown), is illustrated. The interconnect device has two gates 21 which are part of a first level of polycrystalline silicon. The gate oxides 22 and field oxide 23 are silicon dioxide. A second layer 24 of polycrystalline silicon functions as a connector between the transistors. The structure is covered with a suitable dielectric material 25.

In accordance with this invention, layers of polycrystalline silicon are formed in the amorphous state on any conventional substrate contained in electronic devices, e.g. sapphire, glass, silicon dioxide and the like. The preferred method of depositing silicon layers in accordance with this invention is low pressure chemical vapor deposition (LPCVD). For purposes of this invention, the term "amorphous" means a silicon layer grown, for example, by LPCVD at a

temperature between about 560° and 580°C. Such layers will be totally amorphous if measured by Raman, totally amorphous below but slightly crystalline at 580°C. if studied by x-ray, and totally amorphous with embedded crystallites having an average grain size of between about 60 and 120 angstroms if studied by transmission electron microscopy (TEM). The exact nature of the silicon layer may vary somewhat for a given temperature according to factors such as the arrangement of the substrate in the reactor, the geometrical dimensions of the reactor itself, the exact location and tolerance of the thermocouple and the like.

In contrast, layers deposited by LPCVD under similar conditions but at temperatures of 600° to 620°C. have been demonstrated by conventional methods to be fully crystalline and have average grain dimensions of 300 angstroms or more. In addition, annealing such layers produces polycrystalline silicon in a highly disturbed state comprised of partly well and partly poorly crystallized material. The poorly crystallized material, which may be up to 25 percent by weight of such layers, may make them highly undesirable for device applications since they may have highly strained structures which can lead to device defects.

The subject layers of polycrystalline silicon are preferably deposited by conventional LPCVD techniques from a vapor containing silicon, e.g. silane, at 560° to 580°C. utilizing conventional apparatus. In-situ doped layers are prepared, for example, by mixing a suitable dopant such as phosphine with the silicon-containing vapor. While LPCVD techniques utilizing silane as the silicon-containing vapor are preferred in accordance with this invention, other recognized methodologies and materials producing a similar result may be utilized as well.

The layers are annealed at 850° to 1000°C., preferably in an atmosphere of nitrogen containing 0.5 volume percent of oxygen. The small percent of oxygen present is particularly important with layers doped in-situ with phosphorus because it forms a very thin layer of oxide on the surface of the doped silicon which prevents the outdiffusion of the phosphorus. This thin layer of oxide is removed from the surface of the polycrystalline silicon after annealing and prior to subsequent procedures such as patterning of the silicon layer.

Semiconductor devices are significantly improved in accordance with this invention because deposition of the polycrystalline silicon layers in the amorphous state results in markedly improved grain formation upon annealing. The layers have less strain and higher perfection than layers grown in the polycrystalline state. The layers have an exceptional surface smoothness which provides significantly improved interfaces between adjoining layers and, therefore, reduced potential for electrical breakdown. The subject films have very good microhomogeneity and, therefore, may be very precisely lithographically defined. It is unexpected that these advantageous properties are preserved in the subject films after conversion to the polycrystalline state even though annealing produces a significant increase in internal grain size, i.e., to an average size of about 800 angstroms.

The surface roughness of as-deposited and annealed polycrystalline silicon films may be characterized by optical spectroscopy and electron microscopy. In the optical method, a thin film of silver, i.e., 700 to 1000 angstroms thick, is evaporated onto the surface, and the difference in reflectivity is determined by utilizing the methodology described by Cunningham and Braundmeier, Jr. in Phys. Rev. B *14*, 479 (1976).

In accordance with this invention, the root mean square (rms) roughness, σ, of a silicon film grown by LPCVD techniques from silane at 560°C is not more than about 20 angstroms; whereas the rms roughness for a film grown in the same way at 620°C is usually at least 50 angstroms. FIG. 2 is a graph of rms roughness values of polysilicon films annealed at 900° to 1000°C as a function of the deposition temperature. It is clear from the graph that σ-values of about 20 angstroms or less and usually about 15 angstroms or less can only be achieved by LPCVD techniques at deposition temperatures of 580°C. and below.

Thus, contrary to what has been stated in the literature, e.g., Kamins, *J. Electrochem. Soc. 127*, p. 686 (1980), deposition of silicon in the amorphous or amorphous/crystalline states is not to be avoided in the manufacture of semiconductor devices. On the contrary, we have found that complex, multilayer semiconductor devices can be substantially improved by growing silicon layers thereon in the amorphous state due to the exceptional smoothness, lack of strain and microhomogenelty of such layers.

That the subject layers retain their advantageous characteristics through annealing is unexpected because annealing increases grain size. We have observed that the subject layers have an average grain size of about 800 angstroms after annealing, whereas those formed at high temperatures have an average grain size of between 200 and 400 angstroms. That the subject layers unexpectedly retain surface smoothness through annealing is amply shown by the results plotted in FIG. 2, which are of annealed layers and which do not appreciably differ from the results of a similar determination made with as-grown layers.

We have further found that conventional in-situ doping with, for example, phosphorus does not appreciably increase the surface roughness of the subject layers. This is unexpected because it has been recognized that in-situ phosphorus doping enhances grain growth in silicon films. We have observed that, although the volume fraction of crystallites is somewhat higher for an in-situ phosphorus-doped silicon layer deposited at 580°C. than for a corresponding undoped layer, the surface characteristics of both layers are the same. The finding of peak to peak surface roughness, σ_{pp}, values smaller than 50 angstroms

for an in-situ phosphorus-doped, annealed layer is highly unexpected when it is considered that the average grain size as-grown is substantially larger than that of the undoped layer.

The following Examples further illustrate this invention, it being understood that the invention is in no way intended to be limited to the details described therein. In the Examples, all parts and percentages are on a weight basis and all temperatures are in degrees Celsius, unless otherwise stated.

EXAMPLE 1

Deposition of silicon films on 3,000 angstrom thick layers of oxide, thermally grown on (100) silicon substrates, was carried out in a LPCVD reactor in a quartz tube with an inner diameter of 127 mm. The film thickness was typically 0.5 micrometer. The deposition temperature was measured inside the reaction tube. Silicon depositions were carried out at temperatures of 560°, 570°, 580°, 600° and 620° at 350 mtorr, with a 200 cm^3/min flow of silane. As a result of an observed increase in film thickness toward the periphery of the film with increasing temperature, the depositions at 600° and 620° were carried out at 120 millitorr pressure (mtorr) and 50 cm^3/min silane. This improved the radial thickness uniformity and limited the growth rate to about 100 angstroms/min. The silicon films were then thermally annealed in a nitrogen atmosphere at temperatures of 900°, 950° and 1000°.

The films were characterized both as-grown and annealed by Raman and elastic light scattering, optical absorption, UV-reflectivity, x-ray diffraction, electrical conductivity, scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

Using conventional Raman techniques, it was found that the silicon films grown at 560° to 580° were completely amorphous, while those grown at 600° to 620° had sharply increasing crystallinity. The x-ray diffraction and TEM analyses confirmed that the films deposited at 560° were completely amorphous, while those deposited at 580° had small crystallites embedded in the amorphous matrix, and those deposited at 600° and 620° were fully crystalline The annealed material was found to be fully crystalline in all instances.

None of the methods showed any appreciable difference in films annealed at the various temperatures. However, as judged from Raman line width and optical absorption, the films formed at the lower temperatures (560° to 580°) were significantly closer to bulk single-crystal silicon than those deposited at the higher temperatures which were composed of partly well and partly poorly crystallized material. The poorly crystallized material comprised up to about 25 percent by volume of these films. TEM and x-ray analysis showed that the grain size of the film formed at low temperatures increased substantially during annealing, while that grown at high temperatures increased very little. The elastic light scattering results agreed with the results from Raman scattering.

Surface roughness of the silicon films prior to annealing was investigated by electron microscopy and optical spectroscopy using the technique described by Cunningham and Braundmeier. The excitation of surface plasmons amplifies the loss of reflection which could be directly calibrated in terms of σ-values obtained by interferometric methods. For films deposited at 560° and 620°, λ=3500 angstroms, the reflectance (R) from a layer of silver 1000 angstroms thick was R=0.836 and R=0.444, respectively. This clearly shows the loss of reflectance in the film grown in the polycrystalline state at 620°. Using the calibration of Cunningham and Braundmeier, these measurements correlate to an rms roughness σ of less than 15 angstroms for the 560° film and σ=51 angstroms for the 620° film.

TEM micrographs were taken of films grown at 570° and 620° with a 10 to 20 angstroms thick film of platinum evaporated thereon under 45° incidence. It was calculated that the 570° film had a peak-to-peak surface roughness, σ_{pp}, of less than 50 angstroms, whereas that for the 620° film was about 200 to 300 angstroms. As σ_{pp} is several times σ_{rms}, these values correlate well with the roughness values calculated from the optical measurements. In order to determine whether coating of the surface affected the readings, SEM micrographs were taken of the material surface. The same lateral dimensions were found as in the TEM determinations. In both the TEM and SEM studies, it was observed that annealing unexpectedly produced no increase in surface roughness for any of the films.

The electrical conductivity of the films was measured with a test voltage of 50 mV. Measurements were made both in as-grown and annealed films using samples from two separate depositions for each temperature. The spread in conductivity over the annealed films grown at 560°, 570° and 580°, was 5×10^{-7} to 1.9×10^{-6} $(\Omega cm)^{-1}$. For the annealed films deposited at 600° and 620°, samples from one group of depositions showed a small spread in conductivity as had those films grown at the lower temperatures. The second group of depositions, however, showed an extremely large spread of conductivity. It would therefore appear very difficult to obtain films with reproducible material properties at deposition temperatures of 600° and 620°. This observation was borne out by the other tests carried out above.

EXAMPLE 2

Films were deposited in the same manner and at the same five temperatures as in Example 1. The films were doped, in-situ, with phosphorus by adding phosphine to the silane deposition gas with a gas flow ratio of PH_3/SiH_4 of 8×10^{-4}, utilizing one percent phosphine diluted with nitrogen. In order to compensate for the negative influence of phosphine on growth rate and non-

radial uniformity, the deposition pressure was increased to 500 mtorr, and the SiH_4 flow rate was increased to 300 cm^3/min. The films were annealed and characterized as in Example 1.

Using conventional Raman techniques, it was found that the volume percentage of crystallites was somewhat higher and the transition region from amorphous to crystalline lower for the doped films compared to the undoped films of Example 1. The doped films deposited at 580° were amorphous/crystalline, whereas those deposited at 600° were fully crystalline. X-ray diffraction and TEM analysis agreed with the Raman in this regard.

The average grain sizes for in-situ phosphorus doped layers grown at 580° or below was between about 200 and 1000 angstroms as compared with 60 to 120 angstroms for the undoped films. In contrast to the undoped films of Example 1, annealing considerably increased the grain size of all layers, regardless of deposition temperature.

The annealed films were examined by Raman scattering for strain and lattice distortion, critical considerations in device applications. It was found that the doped films had slightly more strain than those grown at low temperature in Example 1, but that doping somewhat reduced the poor crystallization observed in Example 1 for the film deposited at 600°.

The results of elastic light scattering agreed with the Raman scattering, both for as-grown and annealed layers. It was found that the best structures in the doped films were at deposition temperatures not above 570° and that films of lesser quality, but still suitable for certain applications, could be formed at temperatures between 580° and 620°. Above 620°, the quality of the films was unacceptable.

Surface roughness measurements showed that σ-values of about 15 angstroms can only be achieved at deposition temperatures of 580° or less, as was the case with the undoped films of Example 1. In contrast to the films of Example 1, however, is the fact that in-situ phosphorus doped films grown up to 620° still have a surface roughness of less than 30 angstroms which is acceptable for certain applications. TEM micrographs were taken and found to be in good agreement. Overall, it is surprising that σ_{pp} values smaller than 50 angstroms were observed for the doped films when it is considered that the grain size is considerably larger than that of the undoped films.

Conductivity measurements were conducted on the films as in Example 1. The transition deposition temperature was 580°. Films grown below this temperature were amorphous and had low conductivity, i.e., $1\times10^{-2}\ (\Omega cm)^{-1}$, while the films grown above 580° were crystalline and had a high conductivity of $1\times10^{3}\ (\Omega cm)^{-1}$. All annealed films had this conductivity. These values show an average sheet resistivity for a 0.5 micrometer thick film of 20 Ω/sq.

CLAIMS

1. A semiconductor device containing one or more layers of polycrystalline silicon, the improvement wherein said layers have a root mean square roughness of not more than about 20 angstroms.

2. A device in accordance with Claim 1, wherein said layers have a root mean square roughness of about 15 angstroms.

3. A device in accordance with Claim 1 wherein the layers of polycrystalline silicon are formed in the amorphous state and annealed to convert them to the polycrystalline state.

4. A device in accordance with Claim 1, wherein the layers of polycrystalline silicon are formed from a vapor containing silicon.

5. A device in accordance with Claim 4, wherein said vapor is silane.

6. A device in accordance with Claim 4, wherein said layers are formed by low pressure chemical vapor deposition.

7. A device in accordance with Claim 6, wherein said layers are formed at a temperature of from about 560° to about 580°C.

8. A device in accordance with Claim 1, wherein the layers are annealed at a temperature of from about 850° to about 1000°C.

9. A device in accordance with Claim 1, wherein one or more of said layers is doped in-situ.

10. A device in accordance with Claim 9, wherein said layers are formed from a vapor containing silicon which also contains a suitable dopant.

11. A device in accordance with Claim 10, wherein said dopant is phosphine.

12. In a process of forming a semiconductor device comprising, in part, the steps of:

a) depositing a layer of silicon on a substrate;

b) annealing said layer; and

c) forming one or more additional layers of suitable material thereon, the improvement comprising depositing said layer of silicon in the amorphous state and annealing said layer to convert it to the polycrystalline state, said layer having a root mean square roughness of not more than about 20 angstroms.

13. A process in accordance with Claim 12, wherein said layer has a root mean square roughness of about 15 angstroms.

14. A process in accordance with Claim 12, wherein the layer of silicon is formed from a vapor containing silicon.

15. A process in accordance with Claim 14, wherein said vapor is silane.

16. A process in accordance with Claim 14, wherein said layer is formed by low pressure chemical vapor deposition.

17. A process in accordance with Claim 12, wherein the layer is annealed at a temperature of from about 850° to about 1000°C.

18. A process in accordance with Claim 12, wherein said layer is doped in-situ.

19. A process in accordance with Claim 18,

wherein said layer is formed from a vapor containing silicon, said vapor additionally containing a suitable dopant.

20. A process in accordance with Claim 19, wherein said dopant is phosphine.

21. A process of forming a semiconductor device substantially as described hereinbefore with reference to FIGURES 1 and 2 of the accompanying drawing.

22. A semiconductor device substantially as described hereinbefore with reference to FIGURES 1 and 2 of the accompanying drawing.

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